A RASTER COLOR DISPLAY SYSTEM FOR REAL TIME COMPUTER GRAPHICS

A. Malowany and M.D. Levine
McGill University

ABSTRACT

This paper describes a color display system for rendering and animating computer generated images in real time. The design uses a frame buffer, an array of paralleled microprocessor units, and a pipelined architecture with multiple busses. The system is modular permitting the number of video frame buffer planes and microprocessor units to be chosen as needed. Resolutions of 256 x 256 and 512 x 512 are supported on a standard color television monitor. The microprocessor array module uses writable control store for high level graphic instructions and a local memory for macro programs and buffering. Four graphic modes accommodate data packing formats for line generation, areas of uniform color, areas in shaded colors, and frame readback. An interface provides a link to a Z80 microprocessor system and the VAX 780 Computer of the Electrical Engineering Computer Vision and Image Processing Laboratory.

UN SYSTÈME DE TECHNIQUES GRAPHIQUES EN TEMPS RÉEL AVEC AFFICHAGE EN COULEUR

RÉSUMÉ

On décrit un système capable de générer et d'animer des images à partir d'un ordinateur, et ceci en temps réel. Le système utilise une mémoire vidéo, un nombre de microprocesseurs fonctionnant en parallèle, le tout fonctionnant dans un environnement à "bus" multiple qui utilise le principe du pipeline. Le système est modulaire et permet d'augmenter la capacité de la mémoire vidéo, ou le nombre de microprocesseurs, selon les besoins. Deux résolutions (256 x 256 ou 512 x 512 éléments) sont disponibles pour être présentées sur un écran de télévision couleur standard. Les microprocesseurs parallèles offrent une mémoire locale pour les macroprogrammes et tampons, ainsi qu'une mémoire microcode pour les instructions graphiques. Quatre modes d'opération sont disponibles pour la génération de lignes, de surfaces uniformes, de surfaces ombragés, et relecture de l'image. Une interface est responsable pour les communications avec un microprocesseur de type Z-80 et un ordinateur VAX 780. Ce dernier fait partie du laboratoire "Computer Vision and Image Processing" du département de génie électrique de l'université McGill.

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A. Malowany and M.D. Levine
Dept. of Electrical Engineering
McGill University

The Computer Vision and Graphics Laboratory in the Electrical Engineering Department at McGill University includes a variety of computers and image processing peripherals used in undergraduate teaching, and graduate research studies in artificial intelligence, pattern recognition, image processing, scene analysis, computer graphics, optimization and modelling. A Digital Equipment Corp. VAX 11/780 32 bit computer with 512K bytes of memory, 67M byte disc, tape drive, VMS virtual memory operating system with multiusers and multitasking currently supports a dozen interactive terminals. The display systems include Tektronix storage tube displays (models 4002 and 4051), a Sanders vector generator with Kratos beam penetration color display, a Grinnell GMR-27 display having twenty planes of 256 by 256 by 1 bit to support monochrome or RGB color displays with 6 bits of intensity per analog channel. The Grinnell display includes a frame grabber option to digitize images from a TV camera. We are currently developing GRADS, (Graphic Real time Animation Display System) for the display of computer generated images on a raster scanned color monitor. This will be used for teaching, training, studies in real time image animation, modelling, and perception.

The general architecture of the GRADS display system is shown in figure 1. A frame buffer concept was selected offering two advantages. First, the animation rates can be averaged over the complete frame thus smoothing out any computational peaks associated with some parts of the image being displayed. Secondly, the frame buffer is suited to a parallel processing approach. Parallel processing was favoured because of the current availability of relatively cheap microprocessors and because of the simpler technological realization when compared against the "on the fly" serial alternative which demands very high speed processing such as ECL logic. In addition, the parallel approach is inherently flexible due to its modularity, permitting the number of parallelled modules to be increased according to the computational requirements of a particular application. The modularity of the frame buffer also allows the color capability to be expanded as needed.

In order to successfully animate a complex raster image, very large data rates are involved. For example, to display a colored image of 512 by 512 pixels with 5 bits on each of the red, green and blue color channels within 1/30 sec, involves a data rate of 120Mbits/sec. Parallel processing permits this excessively large rate to be divided amongst a number of participating microcomputer modules. Each microcomputer module of the parallel array contributes to the total image by calculating the color information associated with a number of pixels and buffering these results in its local memory. A Graphics Controller Module services the microcomputer array by merging the partial results from each microcomputer local memory buffer into the video frame memory. A TV Sequencer Module continually reads out the contents of the Video Memory to refresh a standard raster scanned RGB color monitor at 30 frames per second. The sequencer module is programmable offering high or low resolutions of 512 or 256 lines per frame and either square or 4 to 3 aspect ratios. The number of video frame planes being accessed is also programmable. A host computer system is responsible for a high level specification of the contribution of each of the microcomputer modules as well as the overall synchronization of the parallel array. The Host Computer Interface Module presents a PDP Unibus port for linking with the VAX 11/780 in the Graphics Laboratory as well as an S100 computer port to a dedicated Cromenco Z80 8 bit microprocessor system having a terminal, floppy disc, parallel and serial interfaces as peripherals. The Z80 system is used mainly for debugging maintenance, and testing although it can also be used to control relatively simple displays.

To exploit concurrency and parallel operation, the GRADS architecture employs many data busses. In addition, the Host Computer Interface, the Graphics Controller, and the TV Sequencer are realized as direct memory access (DMA) devices to liberate the computers from the overhead of moving large blocks of data. To minimize the size of the data blocks envolved in updating the video memory, the Graphics Controller was designed to interpret a header block and accommodate different data packing formats for each of four possible operating modes namely: point or line, solid area, shaded area, and frame readback modes. The point format specifies the chosen color, the number of points to be processed, followed by the stream of image pixel addresses. The solid area format specifies the chosen color, the first and last words of the transfer, as well as the number of consecutive words to be filled between them. The shaded area format specifies the starting address in the video memory, the number of points to be processed, followed by the stream of color words for each of the pixels. The readback format specifies the starting video frame pixel address, the destination address in a microprocessor module, and the number of sequential pixel color words to be read.

The readback mode is intended for maintenance and future real time image processing studies using a frame grabber extension. The point mode can randomly draw either straight lines or arbitrary curves. The solid area mode is useful for filling in large areas with a single color by means of individual horizontal scan lines. It is a highly efficient mode of operation since the video frame updates involve writing on a word basis. The shaded area mode is used to color areas of an image in a similar manner to the solid area mode but using varying color intensities to obtain "shading". The point, shaded and readback modes involve single pixel transactions to each memory plane and are correspondingly less efficient than the solid area mode.

The current realization of the hardware system will now be outlined. To efficiently support the 512 resolution display, 18 bits of addressing are required so a 20 bit Microbus was selected. The current Video Memory planes have 4K 16 bit words of 350 nsec memory. Five AMD2900 4 bit slices are parallelled to form a 20 bit microcomputer module based on a 40 bit micro code word size and a 5MHz clock. The micro code memory consists of 1K words of 100 nsec RAM while the local memory capacity is 4K words of 20 bit, 350 nsec RAM. Thirty-two high speed registers are accessible by the ALU. The 2900 can perform register operations on two arguments and deposit the result in a register within one clock cycle of 200 nsec. The host computer interface permits the downloading of micro coding for the microcomputer operation as well as specially developed high level graphic instruction sets. In operation, the host computer similarly distributes programs consisting of high level instructions and data to microprocessor local memories. Execution of these programs results in output image information being buffered in the microprocessor local memory for the graphics controller to update the video memory.

The performance figures of this display system are difficult to formulate and evaluate theoretically. Because of the video frame buffering, a refresh flicker problem is not expected as the display complexity is increased. Instead, the system accommodates gracefully and the animation update rate decreases from the nominal 33 millisecond value. Rough estimates for animation with the current hardware realization suggest 200 polygons of 1000 pixels for the solid area mode, 100 lines of 100 pixels for the point mode, 15 polygons of 1000 pixels for the shaded area or readback modes. Between two and four microprocessor modules can support this display system depending on the image content and based on estimates for the micro code software. The combined loading of the microprocessor array on the host computer system appears to involve a data rate of approximately 100 KHz. This modest rate will permit the host computer to concentrate its time and computational resources on the problem of animating the display image.

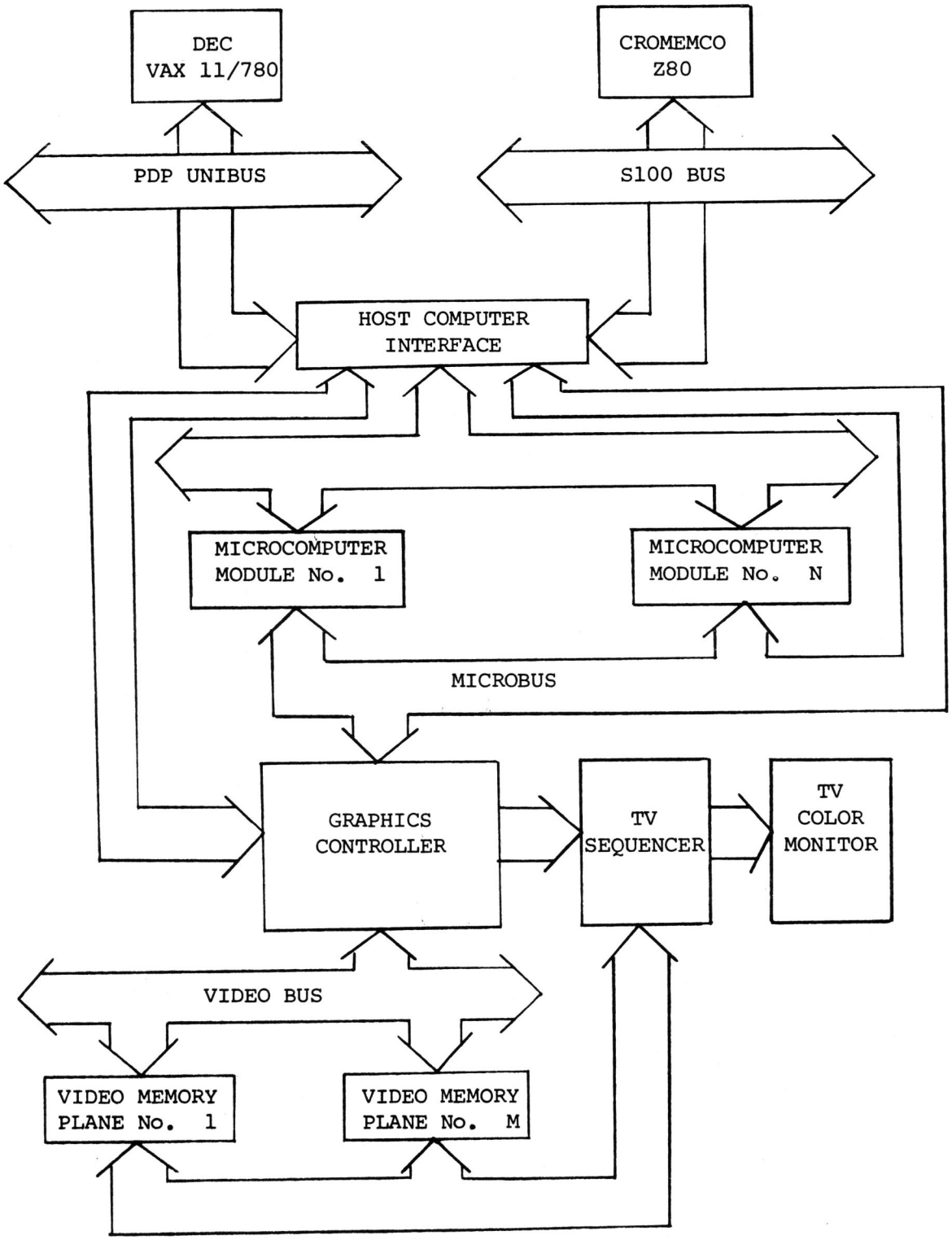

FIGURE 1. THE GRADS ARCHITECTURE

The assembly of all prototype modules and their separate testing is now completed. The integration of the microprocessor system and the graphic controller system is presently underway. The complete system integration is expected during the summer of 79 and the development of micro coding and applications programs will follow.

References

1. Papapetros, A.E., "The Design of a Color Display System for Real Time Animation Using Microprocessors", M.Eng. Thesis, Department of Electrical Engineering, McGill University, 1977.

2. Lamarre, J.Y., "A Multiprocessor Interface for a Graphics Display System", Department of Electrical Engineering, McGill University, February 1979.

3. Ramji, S.A., "A Color Graphics Display System for Real Time Animation Using Microprocessors", Department of Electrical Engineering, McGill University, April 1979.