A LOW COST IMAGE COMPRESSION TEST BED SYSTEM

by

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ABSTRACT

An inexpensive graphics/video raster display processor is described. The system consists of an M6809 microprocessor with 96K high speed memory, 3 D/A converters, 12-bit ALU's and a crystal oscillator. The picture is stored in raster memory in standard Y,U,V components used by the European television system and converted to R,G,B during frame refresh.

KEYWORDS: graphics hardware, raster display, image compression

1. INTRODUCTION

The transmission of photographic colour video images at low data rates (1200 baud for example) has many applications for public information retreival systems such as Telidon. There are many different image compression schemes discussed in the literature, however the hardware decoder cost is the most important parameter which would determine eventual marketability. Our objectives were to design and build a low cost decoder development system and use it to evaluate the various image compression schemes.

A digital picture having a spatial resolution of 256 X 192 pixels and (256)^3 colors requires a 144K byte frame buffer memory. Although data compression techniques allow reducing the size of the frame buffer, very fast hardware is necessary to reconstruct the image during refresh time. A 50% reduction in display memory was obtained by storing the picture information in standard Y,U, and V components used by the European television broadcast system [1] and displaying the Y,U,and V components (converted to R,G and B) with an NTSC composite sync. The Y (luminance component) required 48K of RAM and the remaining 24K was shared by the U and V chrominance components at half the spatial resolution. One bit of the Y memory was reserved as a flag to make the memory compatable with other graphic display systems.

2. YUV System Architecture

The YUV unit consists of five major blocks as shown in Figure 1. The YUV MEMORIES contain 72K bytes of Random Access Memory (RAM) and are address multiplexed to the raster screen as well as the host controller. Static 16K X 1 RAM's with an access time of 55 nsec. were chosen since their high speed would allow individual pixel updating in the time between each display dot on the screen.

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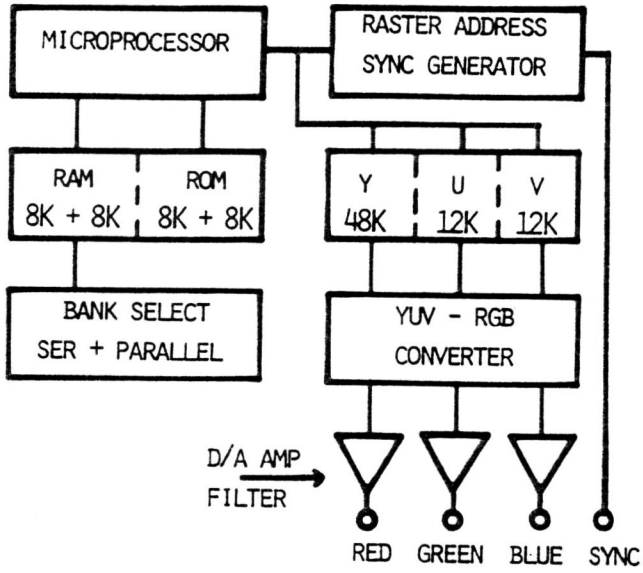

FIGURE 1: BLOCK DIAGRAM OF TEST BED YUV SYSTEM

Horizontal and vertical raster addresses as well as the composite sync pulses are derived from Programmable Read Only Memory (PROM) in the block labelled RASTER ADDRESS & SYNC GENERATOR. The mathematical conversion of the YUV raster memory data into RGB data is accomplished by the YUV - RGB CONVERTER block. The digital RGB data is then converted into analog signals by the D/A FILTER AMP block. The MICROPROCESSOR block includes the RAM/ROM block and the BANK SELECT SER + PARALLEL block and represents any host device or local controller capable of decoding incoming picture data and storing it in video RAM.

An 18-bit address capability is desirable here, although a 16 bit microprocessor with bank switching was implemented in the prototype unit. Figure 2 describes the system memory mapping.

The refresh rate is presently processor limited to approximately 4 frames per second. It is anticipated that 15 frames per second will be achieved with a 68000 microprocessor using 16 bit data lines. Our interest in higher speed is for digital TV studies.

3. D/A FILTER AMP

Data from the YUV-RGB converter is applied to three 8-bit Digital to Analog (D/A) converters. The 6.058 MHz master clock latches the 8-bit R,G and B data bytes into the D/A buffer registers. The deglitched analog output signal settles in 20 nsec. and is applied to an inverting video buffer amplifier which filters and level shifts the Red, Green and Blue (RGB) output voltages. The RGB outputs and the SYNC signal are connected to a standard RGB video monitor for display. The composite blanking pulse is also connected to the D/A converters to disable the output signals during retrace times.

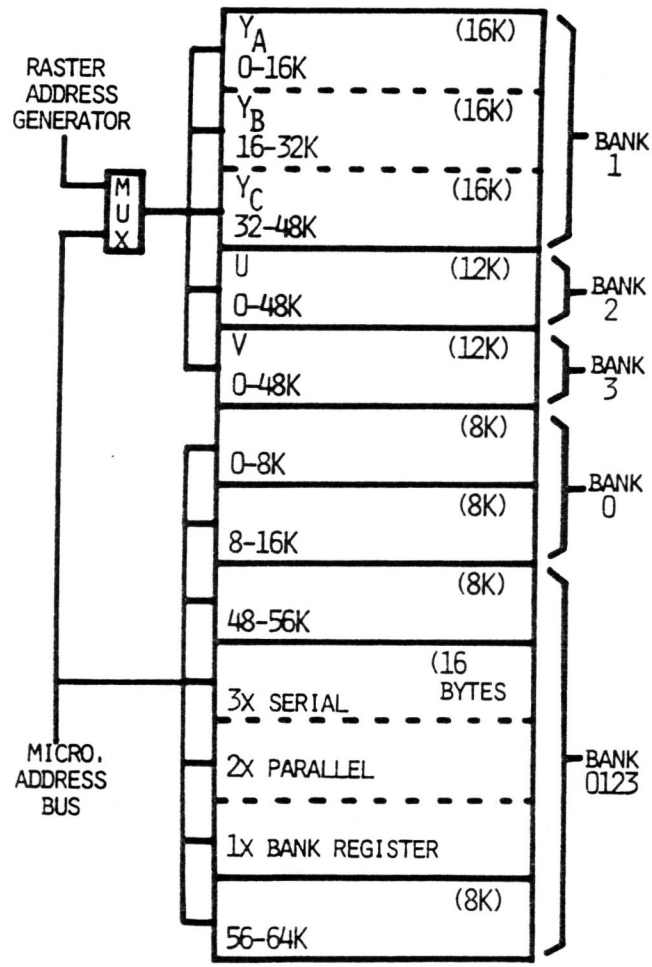

FIGURE 2: MEMORY AND BANK MAPPING

4. YUV to RGB CONVERTER

The conversion from YUV to RGB is accomplished by high speed multiplier ROM's and twelve-bit Arithmetic Logic Units (ALU). The data is input and output latched and adds a delay of only three pixel clock periods. The horizontal timing generator circuitry compensates for this delay such that no display lag is visible on the monitor screen.

The received Y, U, and V digital values were derived from the original R, G, and B signals according to the following equations:

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Y = .299*R + .587*G + .114*B
U = (R-Y) / 1.14
V = (B-Y) / 2.03
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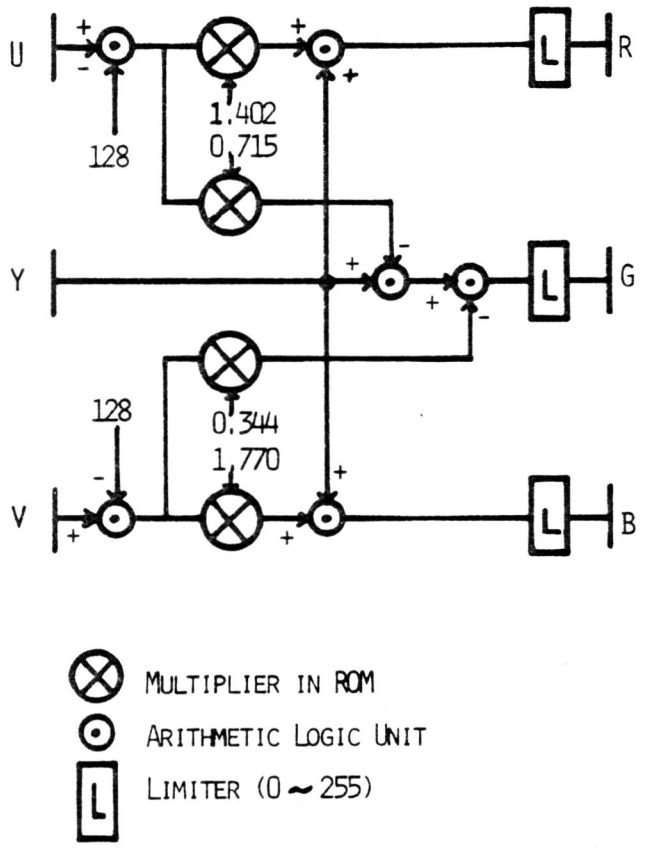

MULTIPLIER IN ROM
ARITHMETIC LOGIC UNIT
LIMITER (0 ~ 255)

FIGURE 3: YUV TO RGB CONVERTER

Analog Y signals range from 0 to 1 volt, while U signals range from -.615 to +.615 volts and V signals range from -.436 to +.436 volts. These YUV values are digitized and scaled so that each component can be represented by a signed 8-bit byte of data. The YUV to RGB conversion must reverse the encoded scaling, correct for signal polarity, and implement the following equations:

```
R = Y + 1.402*U
G = Y - 0.715*U - 0.344*V
B = Y + 1.770*V
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A limiter is applied after the conversion to ensure that 0 <= R,G,B <= 255 for driving the D/A circuitry. Figure 3.

5. RASTER ADDRESS & SYNC GENERATOR

Both the horizontal and vertical synchronization and blanking pulses are derived from a crystal oscillator of 12.115 MHz. (Figure 4). A divide by 2 counter produces the master pixel clock frequency of 6.058 MHz. A divide by 385 counter is used to derive twice the horizontal frequency (31.468 KHz.) then through a further divide by 585 to produce the vertical scanning frequency of 59.94 Hz. The 2X horizontal frequency is divided by 2 and applied to a TTL PROM which generates the correct horizontal sync and blanking pulses. Also connected is an 8-bit counter which sequences through the horizontal raster pixel addresses. The vertical sync and blanking as well as the vertical pixel addresses are similarly derived from the divide by 525 counters. The vertical sync ROM generates pulses for both even and odd fields and is switchable at a field rate by a flip-flop connected to the 59.94 Hz signal.

6. MICROPROCESSOR

This section describes a Motorola 6809 based processor which was used for the prototype YUV system. Although the 6809 has only 16 address lines, it was chosen for compatibility to existing Telidon decoders. A bank switching register was used to address 256K bytes of memory in 4 banks of 64k.

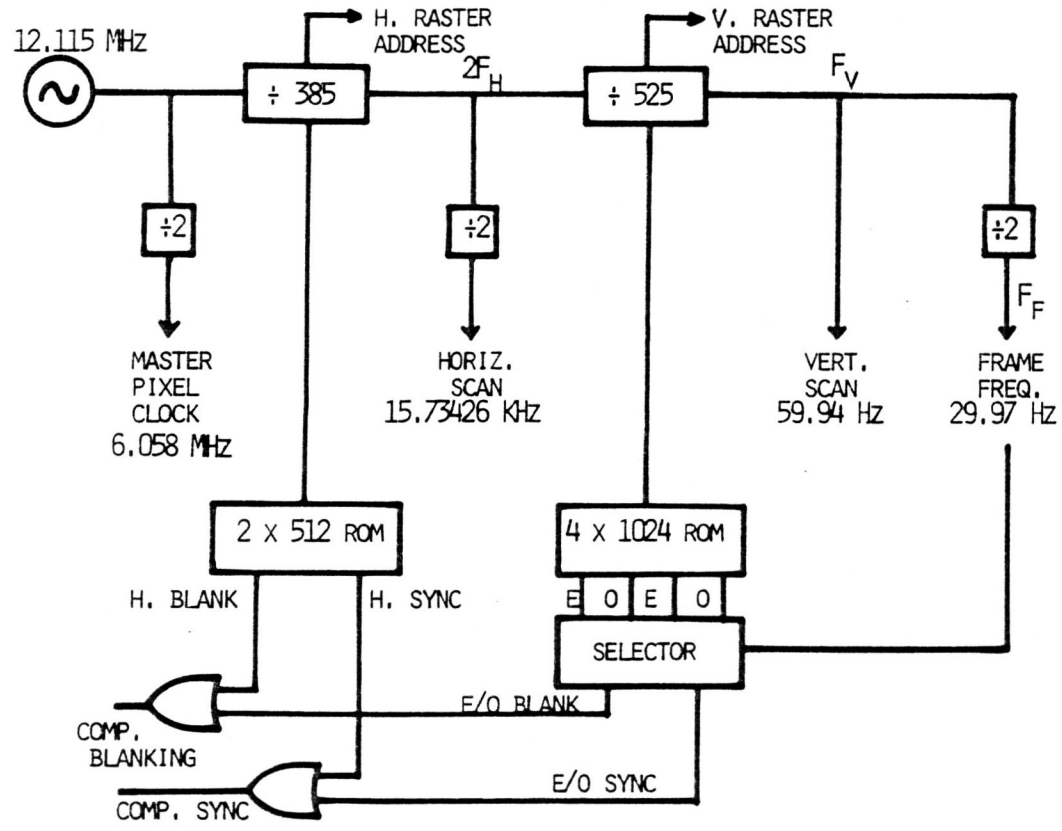

FIGURE 4: RASTER ADDRESS AND SYNC GENERATOR

The largest memory plane is the 48K byte Y bank. The U and V banks only require 12K bytes of storage but they are addressed at a divide by four rate so that they map identically to the Y bank. The fourth bank is extra scratchpad RAM and lookup table ROM. The top 16K bytes of each bank are commonly addressed as 8K RAM and 8K ROM for the system executive. This allows very fast transfers between system RAM and video raster RAM to be handled without executing bank switch instructions.

Input and output consists of three serial ports and two parallel ports all address mapped near the bank switch register. The microprocessor and raster address lines were multiplexed at a pixel clock rate of 6.058 Mhz to access the Y, U and V memories. Between each raster read access of the memories, the microprocessor can execute one complete read or write cycle. Thus the updating of the raster is asynchronous and does not disrupt the screen display.

7. PROTOTYPE TESTBED UNIT

A photograph and funtional overlay (Figure 5) have been included here to show the relative size and complexity of the standalone testbed system. The entire unit was fabricated using wire-wrap techniques and the estimated parts cost was $3000.

8. REFERENCE

[1] Howard Sams and Co.,REFERENCE DATA FOR RADIO ENGINEERS, sixth edition, p.30.34,ISBN 0-672-21218-8, ITT, Indianapolis, Indiana, USA, 1968.

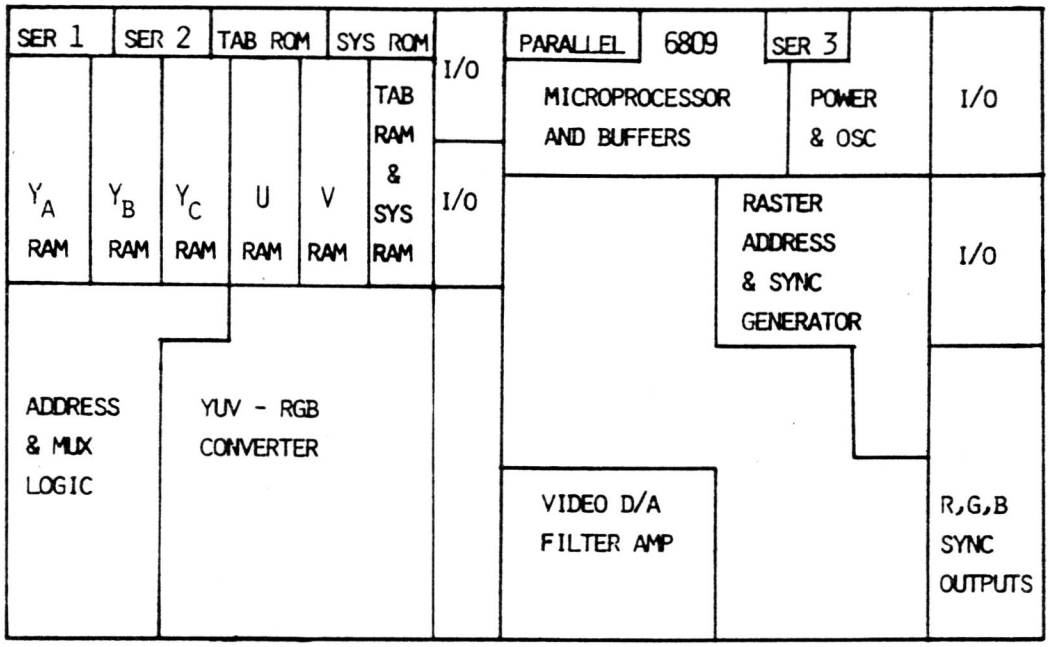

FIGURE 5: WIREWRAP PROTOTYPE PHOTOGRAPH AND LAYOUT